

**IN THE SPECIFICATION:**

Please replace the title on the cover page and at the top of page 2 with the following:  
**CHIP-SCALE PACKAGES HAVING ENCAPSULATED CARRIER BONDS**

**IN THE CLAIMS:**

Claim 2 is amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. Please enter these claims as amended. Also attached is a version with markings to show changes made to the claims.

*Sub D11*

1. (Previously Amended) A chip-scale package comprising:  
a semiconductor die having an active surface having at least one bond pad thereon;  
at least one conductive trace having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;  
at least one conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;  
at least one carrier bond attached to the upper surface of the at least one conductive trace; and  
an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

*B1*

*Sub D21*

2. (Twice Amended) A chip-scale package comprising:  
a semiconductor die having an active surface having a plurality of bond pads thereon;  
a dielectric element having an upper surface and a lower surface, the lower surface of said dielectric element attached to a portion of the active surface of said semiconductor die;